UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,408	03/12/2004	Yan Chong	015114-066900US	7322

26059 7590 06/26/2006

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
STOYNOV, STEFAN	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/799,408	CHONG ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-14 and 17-20* is/are rejected.

7)☒ Claim(s) *4,5,15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/13/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1 and 18 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1 and 18 of copending Application No. 10/779,409 in view of Vogt et al., U.S. Patent No. 6,316,980. All claim limitations in Vogt are disclosed in Figures 1-4.

Claim 1 in copending Application No. 10/779,409 discloses an integrating circuit including all claim limitations of claim 1 in the current Application except a phase detector coupled to an output of the first series of delay elements, a storage circuit coupled to the control block and the output of the first series of delay elements, and a delay circuit coupled to the storage circuit.

Vogt teaches data registers 230 (i.e. storage circuit) coupled to calibrator 250 (i.e. coupled to control block) and to the output of a series of delay elements $214_{1\text{-}L}$.

Vogt further teaches an Edge Detector (i.e. phase detector) coupled to an output of the first series of delay elements (Fig. 2). In Vogt, the described circuit arrangement is used in a memory interface circuit 130 for interfacing DDR memory devices (column 2, lines 57-59) to properly calibrate the delay elements (column 1, lines 31-32). Thus, periodic delay calibration for drift caused by environmental factors is achieved (column 1, lines 20-22).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above described circuit arrangement, as suggested by Vogt with the integrated circuit disclosed in claim 1 of copending Application No. 10/779,409 in order to implement a phase detector coupled to an output of the first series of delay elements, a storage circuit coupled to the control block and the output of the first series of delay elements, and a delay circuit coupled to the storage circuit. One of ordinary skill in the art would be motivated to do so in order to periodically calibrate the drift caused by environmental factors for the delay elements in the integrated circuit.

Claim 18 in copending Application No. 10/779,409 discloses a method including all claim limitations of claim 18 in the current Application except storing the plurality of control signals, receiving a data strobe signal, and delaying the data strobe signal a second duration, the second duration dependent on the plurality of stored control signals.

Vogt teaches locking the delay counter 254 (i.e. the count value representative for the delay control signals is stored within the counter) upon zero phase difference between the reference signal and the delayed reference signal (column 4, lines 7-17), receiving the data strobe signal (Fig. 2, DQS 1-L), and repeatedly delaying the data

strobe signal (i.e. for a second duration) depending on the count value (i.e. dependent on the plurality of stored control signals) (column 4, line 65 – column 5, line 14). In Vogt, the described circuit arrangement and method are used in a memory interface circuit 130 for interfacing DDR memory devices (column 2, lines 57-59) to properly calibrate the delay element (column 1, lines 31-32). Thus, periodic delay calibration for drift caused by environmental factors is achieved (column 1, lines 20-22).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the above described circuit arrangement and method, as suggested by Vogt with the method disclosed in claim 18 of copending Application No. 10/779,409 in order to implement storing the plurality of control signals, receiving a data strobe signal, and delaying the data strobe signal a second duration, the second duration dependent on the plurality of stored control signals. One of ordinary skill in the art would be motivated to do so in order to periodically calibrate the drift caused by environmental factors for the delay elements in the integrated circuit.

This is a provisional obviousness-type double patenting rejection.

Drawings

The drawings are objected to because Figures 1-22 contain hand written text, which is hard to read (e.g. Fig(s) 4, 8, and 14). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must

be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claim 7 and 18 are objected to because of the following informalities:

In claim 7, line 3, the word "to" appears to be missing after the word "coupled".

Similarly, in claim 18, line 5, the word "of" appears to be missing after the word "phase".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 10-14, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Saitoh et al., U.S. patent No. 5,604,775. Saitoh discloses all claim limitations in Figures 1-16.

Regarding claim 10, Saitoh discloses an integrated circuit comprising:

a control circuit (FIG. 3) configured to receive a reference clock (REFERENCE CLOCK) and provide a plurality of control bits (column 4, lines 38-40, Z0-Z9);

a storage circuit 43 coupled to receive and store the plurality of control bits, and further configured to provide the plurality of stored control bits (column 4, lines 16-17, column 3, lines 59-61); and

a delay element (11 and 12) configured to receive the plurality of stored control bits (column 3, lines 59-61).

Regarding claim 11, Saitoh further discloses the integrated circuit wherein the control circuit comprises:

a first series of delay elements 10 configured to receive the reference clock (FIG. 3, REFERENCE CLOCK);

a phase detector 30 configured to compare the phases of the reference clock and an output of the first series of delay elements and provide an output signal (column 3, lines 62-67); and

a counter configured to receive the phase detector output and provide the control bits (column 3, line 67 – column 4, line 24, lines 38-47).

Regarding claim 12, Saitoh further discloses the integrated circuit as per claim 11 wherein a polarity of the phase detector output depends on the relative phase of the

reference clock and the output of the first series of delay elements (column 3, line 67 – column 4, line 14, FIG. 4), and the counter is an up-down counter 42 that counts up when the phase detector output has a first polarity, and counts down when the phase detector output has a second polarity (column 4, lines 43-47, column 8, lines 35-51).

Regarding claim 13, Saitoh further discloses the integrated circuit wherein the storage circuit 43 comprises a plurality of flip-flops, each flip-flop having an input configured to receive and store one of the plurality of control bits, and further configured to provide the stored one of the plurality of control bits to the delay element (column 3, lines 59-61, column 4, lines 38-40).

Regarding claim 14, Saitoh further discloses the integrated circuit as per claim 14 wherein each of the plurality of flip-flops in the storage circuit has a clock input configured to receive the output of the delay element (output of 11 coupled to 46, column 4, lines 22-24, lines 38-40).

Regarding claim 17, Saitoh further discloses the integrated circuit wherein the control circuit is a delay-locked circuit (column 1, lines 32-33, lines 37-40, FIG. 3).

Claims 1, 6-8, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Vogt et al., U.S. Patent No. 6,316,980. Vogt discloses all claim limitation in Figures 1-4.

Regarding claim 1, Vogt discloses an integrated circuit comprising:

a control block comprising 130:

a first series of delay elements 214 coupled to the reference clock input (Fig. 2, Reference Signal through MUX(s) 212 – column 3, lines 34-37, lines 51-54);

a phase detector 252 coupled to the reference clock (Fig. 2, Reference Signal) and an output of the first series of delay elements (column 3, lines 51-59, column 4, lines 2-4); and

a counter 254 coupled to the phase detector 152 and the series of delay elements (column 4, lines 5-8);

a storage circuit 230 coupled to the control block 130 (within control block 130) and the output of the first series of delay elements (column 3, lines 45-47); and

a delay circuit 210 coupled to the storage circuit 230.

Regarding claim 6, Vogt further discloses the integrated circuit wherein the delay circuit is a delay element (column 3, lines 15-16).

Regarding claim 7, Vogt further discloses the integrated circuit as per claim 6 further comprising:

a first register 235_1 having a clock input coupled to an output of the delay circuit 214_1; and a second register 235_2 having a complementary clock input coupled to the output of the delay circuit 214_2 (column 3, lines 45-47).

Regarding claim 8, Vogt further discloses the integrated circuit as per claim 7 wherein the first register has a first input and the second register has a second input, and the first and the second inputs are coupled to a data input (Fig. 2, Data DQ_{1-2}).

Regarding claim 18, Vogt discloses a method of delaying a data strobe signal comprising:

receiving a reference clock signal (column 3, lines 34-37, Fig. 2, Reference Signal);

delaying the reference clock signal a first duration, the first duration dependent on a plurality of control signals (column 3, lines 51-59, column 4, lines 7-9);

comparing the phase of the reference clock signal and the delayed reference clock signal to generate the plurality of control signals (column 4, lines 1-12);

storing the plurality of control signals;

[Vogt inherently discloses storing the plurality of control signals because Vogt discloses locking the delay counter (i.e. the count value representative for the delay control signals is stored within the counter) upon zero phase difference between the reference signal and the delayed reference signal – column 4, lines 7-17]

receiving a data strobe signal (Fig. 2, DQS 1-L); and

delaying the data strobe signal a second duration, the second duration dependent on the plurality of stored control signals (column 4, line 65 – column 5, line 14).

Regarding claim 19, Vogt further discloses the method wherein the plurality of control signals are stored when the received data strobe has been delayed the second duration.

[Vogt inherently discloses plurality of control signals are stored when the received data strobe has been delayed the second duration because Vogt discloses locking the count value (i.e. storing the control signals) is repeated (i.e. more than one time interval with different durations) until the phase difference between the reference signal and the calibration signal is zero – column 4, line 65 – column 5, line 14]

Regarding claim 20, Vogt further discloses the method wherein the plurality of the control signals are stored when an edge of the data strobe signal is not being delayed (column 4, lines 17-21).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vogt et al., U.S. Patent No. 6,316,980 in view of Saitoh et al., U.S. patent No. 5,604,775. Vogt and Saitoh disclose all claim limitations in Figures 1-4 and 1-16 accordingly.

Regarding claim 2, Vogt discloses the integrated circuit as per claim 1 wherein the storage circuit comprises a plurality of flip-flops (column 3, lines 43-44, Fig. 2).

Vogt fails to disclose the flip-flops having an input coupled to the counter in the control block, an output coupled to the delay circuit, and a clock input coupled to an output of the delay circuit.

Saitoh teaches a delay controller 40 and a latch 43 for storing control bits (Z0-Z9) generated by a up/down counter 42, further used as control bits (X0-X6 and Y0-Y2) to adjust the delay for a variable delay line 10 (column 4, lines 15-24, lines 38-40). Saitoh further teaches updating the latch information in the latch by a timing pulse generated by a counter 46 (column 4, lines 22-24, lines 38-40), coupled with the output of the delay line 11 (Fig. 2) (i.e. the latch clock input is coupled to the latch from the output of the delay line through the counter). In Saitoh, the above-described control circuit provides a digital phase locked loop having a reduced jitter (column 1, lines 32-33). Thus, the jitter produced as a result of the variation of delays introduced to the reference clock is avoided (column 1, lines 23-25).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use storing the plurality of control bits into a latch (including a plurality of flip-flops), the control bits generated by a up/down counter coupled to the latch and used for updating the delay for the variable delay line coupled to the latch under a clock signal coupled from the output of the delay line to the latch clock input, as suggested by Saitoh with the integrated circuit disclosed by Vogt in order to implement the flip-flops having an input coupled to the counter in the control block, an output coupled to the delay circuit, and a clock input coupled to an output of the delay circuit. One of ordinary skill in the art would be motivated to do so in order to avoid the jitter produced as a result of the variation of delays introduced to the reference clock supplied to the integrated circuit.

Regarding claim 3, Vogt discloses the integrated circuit as per claim 1.

Vogt fails to disclose a logic gate coupled to an input and the output of the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit.

Saitoh teaches a sequence controller 41 (i.e. logic gate), coupled to the input a and the output of the delay line 10 (trough counters 44, 46, and phase detector 30), further coupled to a latch 43, the latch coupled between the up/down counter 43 and the variable delay line 10. In Saitoh, the above-described control circuit arrangement provides a digital phase locked loop having a reduced jitter (column 1, lines 32-33). Thus, the jitter produced as a result of the variation of delays introduced to the reference clock is avoided (column 1, lines 23-25).

It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the logic gate and above described circuit arrangement, as suggested by Saitoh with the integrated circuit discloses by Vogt in order to implement a logic gate coupled to an input and the output of the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit. One of ordinary skill in the art would be motivated to do so in order to avoid the jitter produced as a result of the variation of delays introduced to the reference clock supplied to the integrated circuit.

Regarding claim 9, Vogt does not specifically state wherein the integrated circuit is a field programmable gate array (FPGA). The examiner takes Official Notice that implementing integrated circuits (ICs) with FPGAs is well known in the art. FPGAs allow for easily changing the IC's hardware parameters by software, thus providing design flexibility, saving cost and time. Accordingly, it would have been obvious to one of

ordinary skill in the art at the time of applicant's invention to implement the integrated circuit disclosed by Vogt with a FPGA. One of ordinary skill in the art would be motivated to do so in order to provide flexible IC design, save cost and time.

Allowable Subject Matter

Claims 4, 5, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 4, the prior art of record fails to disclose or suggest the subject matter of claim 1 "wherein the storage circuit comprises a logic gate coupled to an input of a delay element in the delay circuit and an output of a delay element in the delay circuit, and further coupled to a latch, the latch coupled between the counter in the control circuit and the delay circuit".

Regarding claim 15, the prior art of record fails to disclose or suggest the subject matter of claim 11 "wherein the storage circuit comprises a logic gate configured to receive a signal from an input of a delay element in the second series of delay elements and an output of the second series of delay elements, and further configured to provide an output to a plurality of latches, each latch configured to receive and store one of the plurality of control bits, and further configured to provide the stored one of the plurality of control bits to the delay element".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is (571) 272-4236. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100